Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) Reset circuit comprising a clock signal input for receiving a clock signal consisting of a sequence of clock signal cycles, comprising a data signal input for receiving digital data signals, said digital data signals being encoded in such a manner that at least one signal edge appears per data bit in the data signal, comprising a counting stage being connected to the data signal input and the clock signal input and being designed for counting a number of clock signal cycles, which clock signal cycles appear between a defined number of data signal edges, and comprising comparing means, said comparing means being designed for comparing the number of clock signal cycles counted by the counting stage with a lower limit established to indicate a failure of the clock signal and/or with an upper limit established to indicate a failure of the digital data signals and said comparing means being designed to emit a reset signal, if the number either remains below the lower limit or exceeds the upper limit, depending on the limit value taken for comparison.

2. (previously presented) A data carrier comprising a logic circuit said logic circuit being designed for receiving digital data signals and for producing output data and for receiving a reset signal said reset signal being provided to set the logic circuit into a defined logical state, wherein the data carrier comprising a reset circuit as claimed in claim 1 and wherein the reset signal of the reset circuit being provided to be supplied to the logic circuit.

3. (previously presented) A data carrier as claimed in claim 2, wherein the data carrier comprising a pad for connecting external data input lines, data output lines, clock signal

lines and preferably power supply lines to the reset circuit and the logic circuit respectively.

4. (previously presented) A data carrier as claimed in claim 2, wherein the data carrier comprising a coupling element for contactless transmission of signals and comprising an air interface for processing received signals, wherein the air interface being provided for extracting data signals and clock signals from the received signals and for forwarding the extracted data signals to the reset circuit and the logic circuit respectively.

5. (previously presented) A data carrier as claimed in claim 4, wherein the air interface being designed for extracting electrical energy for supplying the reset circuit and the logic circuit with energy, wherein the extracted electrical energy being preferably buffered intermediately in an energy storage means.

6. (previously presented) A data carrier as claimed in claim 2, wherein the data carrier comprising a subscriber's identification module for a mobile telephone application.

7. (previously presented) A communication device comprising a data carrier as claimed in claim 2.

8. (previously presented) A communication device being designed for communicating with a data carrier as claimed in claim 3, wherein the communication device comprising a coupling element for contactless transmission of signals and an air interface for processing received signals, wherein the air interface being provided for extracting digital data reception signals and clock signals from the received signals and for making the digital data reception signals available for forwarding to the data carrier.

9. (currently amended) A communication device as claimed in claim 8, wherein the air interface comprising a pseudo data generator, wherein said pseudo data generator ~~being~~ is designed for making a pseudo data signal, ~~which~~ wherein said pseudo data signal ~~being~~ is coded in such a way that at least one signal edge occurs per data bit in the pseudo data

signal, available for forwarding to the data carrier, if ~~no signals can be received by~~ the coupling element does not receive any signals from which ~~signals~~ valid data reception signals could be extracted.

10. (currently amended) A communication device as claimed in claim 8, wherein the air interface comprising a pseudo clock signal generator, wherein said pseudo clock signal generator ~~being~~ is designed for making available a pseudo clock signal consisting of a sequence of clock signal cycles for forwarding to the data carrier, if ~~no electromagnetic signals can be received by~~ the coupling element does not receive any electromagnetic signals from which ~~electromagnetic signals~~ valid clock signals could be extracted.

11. (previously presented) A communication device as claimed in claim 7, wherein the communication device being designed as a mobile phone, a personal digital assistant or a personal computer.

12. (currently amended) A reset method for resetting a data carrier and its logic circuit respectively, in a defined logical state, comprising reception of a clock signal consisting of a sequence of clock signal cycles, and comprising reception of digital data signals, said digital data signals being encoded in such a manner that at least one signal edge appears per data bit in the data signal and comprising counting of a number of clock signal cycles, which clock signal cycles appear between a defined number of data signal edges, and comprising comparison of the number of counted clock signal cycles with a lower limit established to indicate a failure of the clock signal and/or with an upper limit established to indicate a failure of the digital data signals and comprising emitting of a reset signal for the logic circuit if the number either remains below the lower limit or exceeds the upper limit depending on the limit value taken for comparison.

13. (new) A communication device being designed for communicating with a data carrier comprising a logic circuit said logic circuit being designed for receiving digital data signals and for producing output data and for receiving a reset signal said reset signal being provided to set the logic circuit into a defined logical state, a reset circuit comprising a clock signal input for receiving a clock signal consisting of a sequence of

clock signal cycles, comprising a data signal input for receiving digital data signals, said digital data signals being encoded in such a manner that at least one signal edge appears per data bit in the data signal, comprising a counting stage being connected to the data signal input and the clock signal input and being designed for counting a number of clock signal cycles, which clock signal cycles appear between a defined number of data signal edges, and comprising comparing means, said comparing means being designed for comparing the number of clock signal cycles counted by the counting stage with a lower limit and/or with an upper limit and said comparing means being designed to emit a reset signal, if the number either remains below the lower limit or exceeds the upper limit, depending on the limit value taken for comparison and wherein the reset signal of the reset circuit being provided to be supplied to the logic circuit, and a pad for connecting external data input lines, data output lines, clock signal lines and preferably power supply lines to the reset circuit and the logic circuit respectively, comprising:

a coupling element for contactless transmission of signals; and

an air interface for processing received signals,

wherein the air interface is provided for extracting digital data reception signals and clock signals from the received signals and for making the digital data reception signals available for forwarding to the data carrier and comprises a pseudo data generator, wherein said pseudo data generator is designed for making a pseudo data signal, wherein said pseudo data signal is coded in such a way that at least one signal edge occurs per data bit in the pseudo data signal, available for forwarding to the data carrier, if the coupling element does not receive any signals from which valid data reception signals could be extracted.